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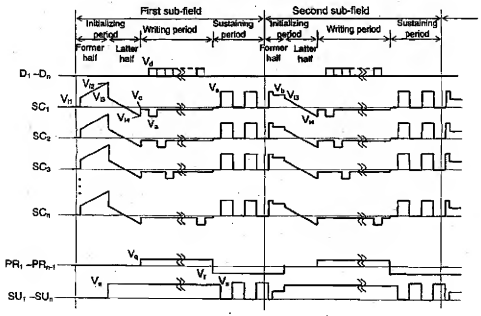
(54) PLASMA DISPLAY PANEL DRIVE METHOD

(57) The initializing period of at least one of a plurality of sub-fields constituting one field is a selective initializing period for selectively initializing discharge cells in which sustain discharge has occurred in the sustaining period of the preceding sub-field. In the sustaining period of the sub-field prior to the sub-field including the selective initializing period, voltage Vr is applied to a priming electrode (PRi) for causing discharge between the priming electrode (PRi) and corresponding scan electrode (SCi) using the priming electrode (PRi) as a cathode.

FIG. 4



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Description

TECNICAL FIELD

[0001] The present invention relates to a method of driving a plasma display panel.

BACKGROUND ART

[0002] A plasma display panel (hereinafter abbreviated as a PDP or a panel) is a display device having excellent visibility and featuring a large screen, thinness and light weight. The systems of discharging a PDP include an alternating-current (AC) type and direct-current (DC) type. The electrode structures thereof include a three-electrode surface-discharge type and an opposite-discharge type. However, the current mainstream is an AC type three-electrode PDP, which is an AC surface-discharge type, because this type of PDP is suitable for higher definition and easy to manufacture.

[0003] Generally, an AC type three-electrode PDP has a large number of discharge cells formed between a front panel and rear panel faced with each other. In the front panel, a plurality of display electrodes, each made of a pair of scan electrode and sustain electrode, are formed on a front glass substrate in parallel with each other. A dielectric layer and a protective layer are formed to cover these display electrodes. In the rear panel, a plurality of parallel data electrodes is formed on a rear glass substrate. A dielectric layer is formed on the data electrodes to cover them. Further, a plurality of barrier ribs is formed on the dielectric layer in parallel with the data electrodes. Phosphor layers are formed on the surface of the dielectric layer and the side faces of the barrier ribs. Then, the front panel and the rear panel are faced with each other and sealed together so that the display electrodes and data electrodes intersect with each other. A discharge gas is filled into an inside discharge space formed therebetween. In a panel structured as above, ultraviolet light is generated by gas discharge in each discharge cell. This ultraviolet light excites respective phosphors to emit R, G, or B color, for color display.

[0004] A general method of driving a panel is a so-called sub-field method: one field period is divided into a plurality of sub-fields and combination of light-emitting sub-fields provides gradation images for display. Now, each of the sub-fields has an initializing period, writing period, and sustaining period.

[0005] In the initializing period, all the discharge cells perform initializing discharge operation at a time to erase the history of wall electric charge previously formed in respective discharge cells and form wall electric charge necessary for the subsequent writing operation. Additionally, this initializing discharge operation serves to generate priming (priming for discharge = excited particles) for causing stable writing discharge.

[0006] In the writing period, scan pulses are sequentially applied to scan electrodes, and write pulses corresponding to the signals of an image to be displayed are applied to data electrodes. Thus, selective writing discharge is caused between scan electrodes and corresponding data electrodes for selective formation of wall electric charge.

[0007] In the subsequent sustaining period, a predetermined number of sustain pulses are applied between scan electrodes and corresponding sustain electrodes. Then, the discharge cells in which wall electric charge are formed by the writing discharge are selectively discharged and light is emitted from the discharge cells.

[0008] In this manner, to properly display an image, selective writing discharge must securely be performed in the writing period. However, there are many factors in increasing discharge delay in the writing discharge: restraints of the circuitry inhibit the use of high voltage for write pulses; and phosphor layers formed on the data electrodes make discharge difficult. For these reasons, priming for generating stable writing discharge is extremely important.

[0009] However, the priming caused by discharge rapidly decreases as time elapses. This causes the following problems in the method of driving a panel described above. In writing discharge occurring long time after the initializing discharge, priming generated in the initializing discharge is insufficient. This insufficient priming causes a large discharge delay and unstable wiring operation, thus degrading the image display quality. Additionally, when long wiring period is set for stable wiring operation, the time taken for the writing period is too long.

[0010] Proposed to address these problems are a panel and method of driving the panel in which auxiliary discharge electrodes are provided and discharge delay is minimized using priming caused by auxiliary discharge (see Japanese Patent Unexamined Publication No. 2002-297091, for example).

[0011] On the other hand, as a method of driving a panel, a so-called high-contrast driving method is proposed and put into actual use. In this method, the number of times of light emission in an initializing discharge unrelated to gradation representation is minimized to improve a contrast ratio (see Japanese Patent Unexamined Publication No. 2000-242224, for example).

[0012] In the above high-contrast driving method, one field is made of a plurality of sub-fields, each including an initializing period, writing period, and sustaining period. Initializing operations performed in the initializing period include an all-cell initializing operation for initializing all the discharge cells, and a selective initializing operation for selectively initializing the discharge cells in which discharge has occurred. The all-cell initializing operation is performed only in the initializing period in the first sub-field, for example. In the other sub-fields, the selective initializing operation is performed.

[0013] As described above, the initializing operation

performed in the most of the sub-fields in the plurality of sub-fields is the selective initializing operation for causing discharge only in the discharge cells in which sustain discharge has occurred. Therefore, initializing light emission unrelated to gradation representation is only once in one field, i.e. the all-cell initializing operation in the first sub-field. Further, the light emission is weak light emission caused by ramp waveform voltage. For this reason, an image with high contrast can be obtained.

[0014] Future PDPs tend to have an increasing number of discharge cells necessitated by a larger screen size and higher definition, or an increasing number of sub-fields for achieving smoother image quality. With these trends, in spite of an increase in the number of writing operations, the time spent for the writing operation decreases. Thus, the time allocated for one writing operation tends to be shortened. For this reason, techniques of decreasing discharge delay in the writing operation are more and more important in the future. On the other hand, contrast must further be improved for more powerful image representation. These demands require integration of these techniques: achieving high contrast and high-speed writing operation at the same time.

[0015] The present invention addresses these problems and aims to provide a method of driving a plasma display panel capable of achieving high contrast and high-speed writing operation.

DISCLOSURE OF THE INVENTION

[0016] The method of driving a plasma display panel of the present invention includes applying, to priming electrodes, a voltage for causing discharge between the priming electrodes and scan electrodes using the priming electrodes as cathodes, prior to priming discharge in a writing period in a sub-field having a selective initializing period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Fig. 1 is a sectional view showing an example of a panel used for an exemplary embodiment of the present invention.

Fig. 2 is a schematic perspective view showing a structure of a rear substrate side of the panel.

Fig. 3 is a diagram showing an arrangement of electrodes in the panel.

Fig. 4 is a diagram showing a driving waveform in a method of driving the panel.

Fig. 5 is a diagram showing another driving waveform in a method of driving the panel.

Fig. 6 is diagram showing an example of a circuit block of a driver for implementing the method of driving the panel.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0018] A method of driving a plasma display panel in accordance with an exemplary embodiment of the present invention is described hereinafter with reference to the accompanying drawings.

Exemplary Embodiment

[0019] Fig. 1 is a sectional view showing an example of a panel used for the exemplary embodiment of the present invention. Fig. 2 is a schematic perspective view showing the structure of the rear substrate side of the panel.

[0020] As shown in Fig. 1, front substrate 1 and rear substrate 2 both made of glass are faced with each other to sandwich a discharge space therebetween. A mixed gas of neon and xenon for radiating ultraviolet light by discharge is filled in the discharge space.

[0021] On front substrate 1, a plurality of pairs of scan electrode 6 and sustain electrode 7 are formed in parallel with each other. Scan electrodes 6 and sustain electrodes 7 are alternately arranged in pairs like sustain electrode 7 - scan electrode 6 - scan electrode 6 - sustain electrode 7, etc. Scan electrode 6 and sustain electrode 7 are made of transparent electrodes 6a and 7a, and metal buses 6b and 7b formed on transparent electrodes 6a and 7a, respectively. Now, between one scan electrode 6 and the other scan electrode 6, and one sustain electrode 7 and the other scan electrode 7, light-absorbing layers 8, each made of a black material, are provided. Projection 6b' of metal bus 6b in one of a pair of scan electrodes 6 projects onto light-absorbing layer 8. Dielectric layer 4 and protective layer 5 are formed to cover these scan electrodes 6, sustain electrodes 7, and light-absorbing layers 8.

[0022] On rear substrate 2, a plurality of data electrodes 9 is formed in parallel with each other. Dielectric layer 15 is formed to cover these data electrodes 9. Further on the dielectric layer, barrier ribs 10 for partitioning the discharge space into discharge cells 11 are formed. As shown in Fig. 2, each barrier rib 10 is made of vertical walls 10a extending in parallel with data electrodes 9, and horizontal walls 10b for forming discharge cells 11 and forming clearance 13 between discharge cells 11. In every other one of clearances 13, priming electrode 14 is formed in the direction orthogonal to data electrodes 9, to form priming space 13a. On the surface of dielectric layer 15 corresponding to discharge cells 11 partitioned by barrier ribs 10 and the side faces of barrier ribs 10, phosphor layers 12 are provided. However, no phosphor layer 12 is formed on the side of clearances 13.

[0023] When front substrate 1 is faced and sealed with rear substrate 2, each projection 6b' of metal bus 6b in scan electrode 6 formed on front substrate 1 that projects onto light-absorbing layer 8 is positioned in par-

allel with corresponding priming electrode 14 on rear substrate 2 and faced therewith to sandwich priming space 13a. In other words, the panel shown in Figs. 1 and 2 is structured to perform priming discharge between projections 6b' formed on the side of front substrate 1 and priming electrodes 14 formed on the side of rear substrate 2.

[0024] In Figs. 1 and 2, dielectric layer 16 is further formed to cover priming electrodes 14; however, this dielectric layer 16 need not be formed necessarily.

[0025] Fig. 3 is a diagram showing an arrangement of electrodes in the panel used for the exemplary embodiment of the present invention. M columns of data electrodes D_1 to D_m (data electrodes 9 in Fig. 1) are arranged in the column direction. N rows of scan electrodes SC_1 to SC_n (scan electrodes 6 in Fig. 1), and n rows of sustain electrodes SU_1 to SU_n (sustain electrodes 7 in Fig. 1) are alternately arranged in pairs in the row direction like sustain electrode SU_1 - scan electrode SC_1 - scan electrode SC_2 - sustain electrode SU_2, etc. In this embodiment, n/2 rows of priming electrodes PR_1, PR_3, etc. (priming electrode 14 in Fig. 1) are arranged to be faced with corresponding projections 6b' of scan electrodes SU_1, SU_3, etc. of the odd-numbered rows.

[0026] Thus, m × n discharge cells C_{ij} (discharge cells 11 in Fig. 1), each including a pair of scan electrode SC_i and sustain electrode SU_i (i = 1 to n) and one data electrode D_j (j = 1 to m), are formed in the discharge space. N/2 rows of priming spaces PS_p (priming space 13a in Fig. 1), each including projection 6b' of scan electrode SC_p (p = odd number) and priming electrode PR_p, are formed.

[0027] Next, a driving waveform for driving the panel and timing of the driving waveform are described.

[0028] Fig. 4 is a diagram showing a driving waveform in the method of driving the panel used for the exemplary embodiment of the present invention. In this embodiment, one field period is made of a plurality of sub-fields, each including an initializing period, writing period, and sustaining period. The initializing period in the first sub-field is an all-cell initializing period for initializing all the discharge cells related to image display. In the initializing periods in the second sub-field or after, a selective initializing operation for selectively initializing the discharge cells in which sustain discharge has occurred in the preceding sub-field is performed. Descriptions are given on the basis of these ideas.

[0029] In the former half of the initializing period in the first sub-field, each of data electrodes D_1 to D_m, sustain electrode SU_1 to SU_n, and priming electrodes PR_1 to PR_{n-1} is held at 0 (V). Applied to each of scan electrodes SC_1 to SC_n is a ramp waveform voltage gradually increasing from a voltage of V_{i1} not larger than discharge-starting voltage across the scan electrodes and sustain electrodes SU_1 to SU_n to a voltage of V_{i2} exceeding the discharge-starting voltage. While the ramp waveform voltage increases, first weak initializing discharge occurs between scan electrodes SC_1 to SC_n, and sustain electrodes SU_1 to SU_n, data electrodes D_1 to D_m, and priming electrodes PR_1 to PR_{n-1}. Thus, negative wall voltage accumulates on scan electrodes SC_1 to SC_n, and positive wall voltage accumulates on data electrodes D_1 to D_m, sustain electrodes SU_1 to SU_n, and priming electrodes PR_1 to PR_{n-1}. Now, the wall voltage on the electrodes is the voltage generated by the wall charge accumulating on the dielectric layers covering the electrodes.

[0030] In the latter half of the initializing period in the first sub-field, each of sustain electrode SU_1 to SU_n is held at a positive voltage of Ve. Applied to each of scan electrodes SC_1 to SC_n is a ramp waveform voltage gradually decreasing from a voltage of V_{i3} not larger than discharge-starting voltage across the scan electrodes and sustain electrodes SU_1 to SU_n to a voltage of V_{i4} exceeding the discharge-starting voltage. During this application of the ramp voltage, second weak initializing discharge occurs between scan electrodes SC_1 to SC_n, and sustain electrodes SU_1 to SU_n, data electrodes D_1 to D_m, and priming electrodes PR_1 to PR_{n-1}. Then, the negative wall voltage on scan electrodes SC_1 to SC_n and the positive wall voltage on sustain electrodes SU_1 to SU_n are weakened. The positive wall voltage on data electrodes D_1 to D_m is adjusted to a value appropriate for writing operation. The positive wall voltage on priming electrodes PR_1 to PR_{n-1} is also adjusted to a value appropriate for priming operation. Thus, the all-cell initializing operation for initializing all the discharge cells related to image display is completed.

[0031] In the writing period, scan electrodes SC_1 to SC_n are once held at a voltage of Vc. Then, a voltage of Vq substantially equal to voltage change Vc - V_{i4} is applied to priming electrodes PR_1 to PR_{n-1}.

[0032] Next, scan pulse Va is applied to scan electrode SC_1 of the first row. Then, the potential difference between priming electrode PR_1 and projection 6b' of scan electrode SC_1 is addition of Vq - Va and the wall voltage on priming electrode PR_1. Thus, the potential difference exceeds the discharge-starting voltage and priming discharge occurs. The priming diffuses inside of discharge cells $C_{1,1}$ to $C_{1,m}$ in the first row and discharge cells $C_{2,1}$ to $C_{2,m}$ in the second row. Because the priming space PS_1 is structured to easily discharge as described above, high-speed and stable priming discharge with a small discharge delay can obtained. This discharge accumulates positive wall voltage on priming electrode PR_1.

[0033] At the same time, positive write pulse voltage Vd is applied to data electrode D_k (k being an integer ranging from 1 to m) corresponding to the signal of an image to be displayed in the first row, among data electrodes D_1 to D_m. Then, discharge occurs at the intersection of data electrode D_k to which write pulse voltage Vd has been applied and scan electrode SC_1. This discharge develops to the discharge between sustain electrode SU_1 and scan electrode SC_1 in corresponding discharge cell $C_{1,k}$. Then, positive voltage accumulates on

scan electrode SC_1 and negative voltage accumulates on sustain electrode SU_1 in discharge cell $C_{1,k}$. Thus, the writing operation in the first row is completed.

[0034] Now, in the writing operation in the first row, writing is performed and the priming discharge is caused with scanning of scan electrode SC_1 of the first row. The writing discharge in discharge cell $C_{1,k}$ occurs with the priming supplied from the priming discharge that has occurred between scan electrode SC_1 and priming electrode PR_1. For this reason, although there is a delay in starting the priming, stable discharge with a small discharge delay can be obtained after the supply of the priming.

[0035] Next, scan pulse voltage Va is applied to scan electrode SC_2 of the second row. At the same time, positive write pulse voltage Vd is applied to data electrode D_k corresponding to the signal of the image to be displayed in the second row, among data electrodes D_1 to D_m. Then, discharge occurs at the intersection of data electrode D_k and scan electrode SC_2. This discharge develops to the discharge between sustain electrode SU_2 and scan electrode SC_2 in corresponding discharge cell $C_{2,k}$. Then, positive voltage accumulates on scan electrode SC_2 and negative voltage accumulates on sustain electrode SU_2 in discharge cell $C_{2,k}$. Thus, the writing operation in the second row is completed.

[0036] Now, the writing operation in discharge cell $C_{2,k}$ of the second row is performed with sufficient priming already supplied from the priming discharge that has occurred between scan electrode SC_1 and priming electrode PR_1. For this reason, stable discharge with an extremely small discharge delay in the writing discharge can be obtained.

[0037] In the similar manner, the writing operations are performed in discharge cells including $C_{n,k}$ and the writing operations are completed.

[0038] In the sustaining period, after scan electrodes SC_1 to SC_n and sustain electrodes SU_1 to SU_n are reset to 0 (V) once, a negative voltage of Vr is applied to priming electrodes PR_1 to PR_{n-1}. Thereafter, a positive sustain pulse voltage of Vs is applied to scan electrodes SC_1 to SC_n. At this time, in the voltage on scan electrode SC_i and sustain electrode SU_j in discharge cell C_{ij} in which writing discharge has occurred, the wall voltage accumulating on scan electrode SC_i and sustain electrode SU_j is added to sustain pulse voltage Vs. For this reason, the voltage exceeds the discharge-starting voltage and sustain discharge occurs. In a similar manner, by alternately applying sustain pulses to scan electrodes SC_1 to SC_n and sustain electrodes SU_1 to SU_n, sustain discharge operations are successively performed in discharge cell C_{ij} in which the writing discharge has occurred, the number of times of sustain pulses.

[0039] At this time, discharge also occurs between priming electrode PR_i and scan electrode SC_i corresponding to priming electrode PR_i, using priming electrode PR_i as a cathode. Thus, wall charge having a value depending on potential difference Vs - Vr accumulates on priming electrode PR_i. At this time, at the larger difference between voltage Vs and voltage Vr, the larger positive wall voltage accumulates on priming electrode PR_i.

[0040] In the former half of the initializing period in the second sub-field, a pulse with a small width that increases from 0 (V) to voltage Vs once and promptly decreases to voltage Vb is applied to scan electrodes SC_1 to SC_n. At the same time, a pulse having a small width that decreases from voltage Vs to 0 (V) once and promptly increases to voltage Vb is applied to sustain electrodes SU_1 to SU_n. In the latter half of the initializing period, application of a ramp waveform voltage gradually decreasing voltage V_{i3} to voltage V_{i4} weakens the excessive wall charge. This performs initializing discharge only in the discharge cells in which sustain discharge has occurred, erases the wall charge accumulated by the sustain discharge, and adjusts the positive wall voltage on data electrodes D_1 to D_m to a value appropriate for writing operation and the positive wall voltage on priming electrodes PR_1 to PR_{n-1} to a value appropriate for priming operation.

[0041] The operations in the subsequent writing and sustaining periods are the same as those in the first subfield, and thus the description thereof is omitted.

[0042] As described above, the initializing operation performed in the second sub-field or after is selective initializing operation for causing discharge only in the discharge cells in which sustain discharge has occurred. Therefore, light emission unrelated to gradation representation is only once in one field, i.e. the all-cell initializing operation in the first sub-field. Further, because the light emission is weak light emission caused by the ramp waveform voltage, an image with high contrast can be displayed.

[0043] Further, unlike the writing discharge depending only on the priming in the initializing discharge in accordance with a conventional driving method, the writing discharge of the method of driving a panel in accordance with this embodiment of the present invention is performed with sufficient priming supplied from the priming discharge that has occurred during or immediately before the writing operation in respective discharge cells. This can achieve high-speed and stable writing discharge with a small discharge delay, and display a high-quality image.

[0044] Additionally, electrodes in priming spaces 13a are priming electrodes 14 and scan electrodes 6 only. This also gives an advantage of stable action of the priming discharge itself because the priming discharge is unlikely to cause other unnecessary discharge, e.g. incorrect discharge involving the sustain electrodes.

[0045] Now, to give the reason why the present invention enables high-speed writing while achieving high contrast, the above operations are described again from the viewpoint of wall charge on the priming electrodes.

[0046] First, in the former half of the initializing period

in the first sub-field, excessive and unnecessary positive wall voltage is formed on priming electrodes PR_1 to PR_{n-1} once. In the latter half of the initializing period, the excessive portion of the wall voltage is reduced and adjusted to a value appropriate for priming operation.

[0047] In the writing period, the adjusted positive wall voltage is used to cause priming discharge. This discharge extinguishes the positive wall voltage on priming electrodes PR_1 to PR_{n-1}.

[0048] In the sustaining period, negative voltage Vr applied to priming electrodes PR_1 to PR_{n-1} is added to voltage Vs applied to scan electrodes SC_1 to SC_n, and strong discharge occurs using priming electrodes PR_1 to PR_{n-1} as cathodes. Thus, excessive positive wall voltage is formed on priming electrodes PR_1 to PR_{n-1} again.

[0049] In the former half of the initializing period In the second sub-field, because a potential difference larger than Vs - Vr is not applied across scan electrodes SC_1 to SC_n and priming electrodes PR_1 to PR_{n-1}, no discharge occurs therebetween. However, in the sustaining period immediately before the former half of the initializing period, excessive positive wall voltage is formed on priming electrodes PR_1 to PR_{n-1}. For this reason, in the subsequent latter half of the initializing period, the excessive portion of the wall voltage is reduced and adjusted to a value of the wall voltage appropriate for the subsequent priming operation.

[0050] As described above, because no discharge occurs to form excessive positive wall voltage on priming electrodes PR_1 to PR_{n-1} in the selective initializing period, excessive positive wall voltage must be formed on priming electrodes PR_1 to PR_{n-1} before the latter half of the selective initializing operation. Therefore, as described above, a negative voltage is applied to priming electrodes PR_1 to PR_{n-1} to cause strong discharge between the priming electrodes and corresponding scan electrodes SC_1 to SC_n using priming electrodes PR_1 to PR_{n-1} as cathodes and to form excessive positive wall voltage on priming electrodes PR_1 to PR_{n-1}, in the sustaining period of the sub-field prior to a sub-field including a selective initializing period. This can achieve high contrast and high-speed writing at the same time.

[0051] Fig. 5 shows another waveform in the method of driving the panel used for the exemplary embodiment of the present invention. In Fig. 5 (a), voltage Vr for causing discharge using priming electrodes PR_1 to PR_{n-1} as cathodes is applied to priming electrodes PR_1 to PR_{n-1} only in the beginning of the sustaining period in the sub-field prior to a sub-field including a selective initializing period. In this case, application of first sustain pulse voltage Vs to scan electrodes SC_1 to SC_n causes discharge using priming electrodes PR_1 to PR_{n-1} as cathodes. In Fig. 5 (b), voltage Vr is applied to priming electrodes PR_1 to PR_{n-1} in an intermediate portion of the sustaining period. In this case, application of sustain pulse voltage Vs to scan electrodes SC_1 to SC_n causes discharge using priming electrodes PR_1 to PR_{n-1} as cathodes. In Fig. 5 (c), voltage Vr is applied to priming electrodes PR_1 to PR_{n-1} in the former half of the selective initializing period. In this case, application of pulse voltage Vs having a small width to scan electrodes SC_1 to SC_n causes discharge using priming electrodes PR_1 to PR_{n-1} as cathodes.

[0052] Even application of driving waveforms shown in Fig. 5 (a), (b), or (c), or similar ones to priming electrodes PR_1 to PR_{n-1} can provide effects similar to those of the driving method in accordance with the exemplary embodiment of the present invention.

[0053] Incidentally, because respective electrodes of an AC type PDP are surrounded by the dielectric layers and insulated from the discharge space. For this reason, direct-current components make no contribution to discharge itself. Therefore, of course, even the use of a waveform in which direct-current components are added to the driving waveform of the exemplary embodiment of the present invention can provide similar effects.

[0054] In the description of this exemplary embodiment, in a plurality of sub-fields constituting one field, the first sub-field includes an all-cell initializing period, and the second sub-field or after includes a selective initializing period. However, the present invention can be implemented even when one field includes arbitrary combinations of sub-fields each having an all-cell initializing period and sub-fields each having a selective initializing period.

[0055] Fig. 6 is a diagram showing an example of a circuit block of a driver for implementing the method of driving the panel used for the exemplary embodiment. Driver 100 of the exemplary embodiment of the present invention includes: video signal processor circuit 101, data electrode driver circuit 102, timing controller circuit 103, scan electrode driver circuit 104 and sustain electrode driver circuit 105, and priming electrode driver circuit 106. A video signal and synchronizing signal are fed into video signal processor circuit 101. Responsive to the video signal and synchronizing signal, video signal processor circuit 101 outputs a sub-field signal for controlling whether or not to light each sub-field, to data electrode driver circuit 102. The synchronizing signal is also fed into timing controller circuit 103. Responsive to the synchronizing signal, timing controller circuit 103 outputs a timing control signal to data electrode driver circuit 102, scan electrode driver circuit 104, sustain electrode driver circuit 105, and priming electrode driver circuit 106.

[0056] Responsive to the sub-field signal and the timing control signal, data electrode driver circuit 102 applies a predetermined driving waveform to data electrodes 9 (data electrodes D_1 to D_m in Fig. 3) in the panel. Responsive to the timing control signal, scan electrode driver circuit 104 applies a predetermined driving waveform to scan electrodes 6 (scan electrodes SC_1 to SC_n in Fig. 3) in the panel. Responsive to the timing control signal, sustain electrode driver circuit 105 applies a predetermined driving waveform to sustain electrodes 7

(sustain electrodes SU_1 to SU_n in Fig. 3) in the panel. Responsive to the timing control signal, priming electrode driver circuit 106 applies a predetermined driving waveform to priming electrodes 14 (priming electrodes PR_1 to PR_n in Fig. 3) in the panel. Necessary electric power is supplied to data electrode driver circuit 102, scan electrode driver circuit 104, sustain electrode driver circuit 105, and priming electrode driver circuit 106 from a power supply circuit (not shown).

[0057] The above circuit block can constitute a driver for implementing the method of driving the panel of the exemplary embodiment.

[0058] As described above, the present invention can provide a method of driving a plasma display panel capable of achieving high contrast and stable and high-speed writing operation.

INDUSTRIAL APPLICABILITY

[0059] As described above, the method of driving a plasma display panel of the present invention can achieve high contrast and stable and high-speed writing operation. Thus, the present invention is useful as a method of driving a plasma display panel.

Claims

1. A method of driving a plasma display panel comprising a plurality of scan electrodes and sustain electrodes arranged in parallel with each other, and a plurality of data electrodes arranged in a direction intersecting the scan electrodes, in which one field period is made of a plurality of sub-fields, each including an initializing period, writing period, and sustaining period, the method comprising:

   providing a plurality of priming electrodes in parallel with the scan electrodes, the priming electrodes generating priming discharge between the priming electrodes and the corresponding scan electrodes;
   providing at least one sub-field including a selective initializing period for selectively initializing discharge cells in which sustain discharge has occurred in a sustaining period of a preceding sub-field, in the plurality of sub-fields; and
   applying, to the priming electrodes, a voltage for causing discharge between the priming electrodes and the scan electrodes using the priming electrodes as cathodes, prior to priming discharge in a writing period in the sub-field including the selective initializing period.

2. The method of driving a plasma display panel of claim 1, wherein the voltage for causing discharge using the priming electrodes as cathodes is applied to the priming electrodes in a specified period in a sustaining period of a sub-field prior to the sub-field including at least the selective initializing period.

3. The method of driving a plasma display panel of claim 1, wherein the voltage for causing discharge using the priming electrodes as cathodes is applied to the priming electrodes in a specified period at least in the selective initializing period.

FIG. 1

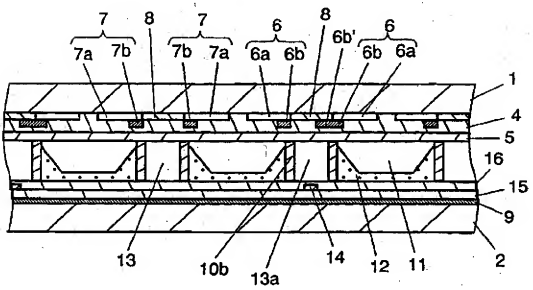

7
8
7
6
8
6
7a
7b
7b
7a
6a
6b
6b'
6b
6a
1
4
5
16
15
9
13
10b
13a
14
12
11
2

FIG. 2

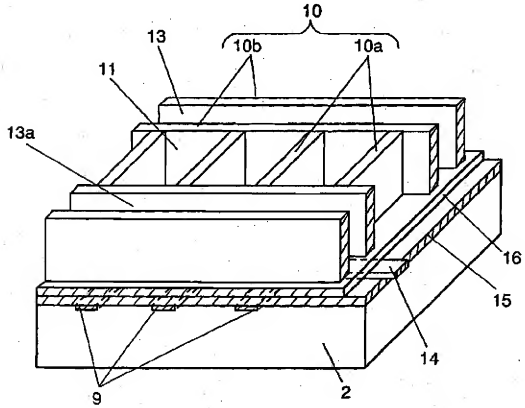

10
13
10b
10a
11
13a
16
15
14
9
2

FIG. 3

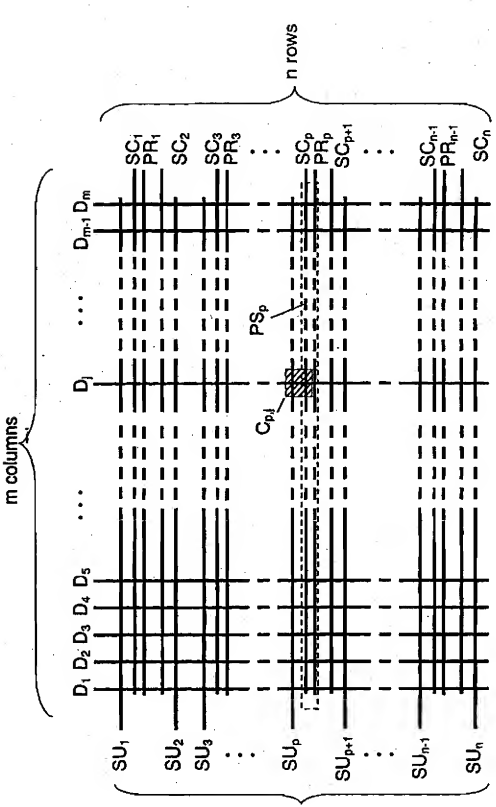

m columns
n rows
n rows
D1 D2 D3 D4 Ds ... Dj ... Dm-1 Dm
SU1 SU2 SU3 ... SUp SUp+1 ... SUn-1 SUn
SC1 PR1 SC2 SC3 PR3 ... SCp PRp SCp+1 ... SCn-1 PRn-1 SCn
PSp
Cpj

FIG. 4

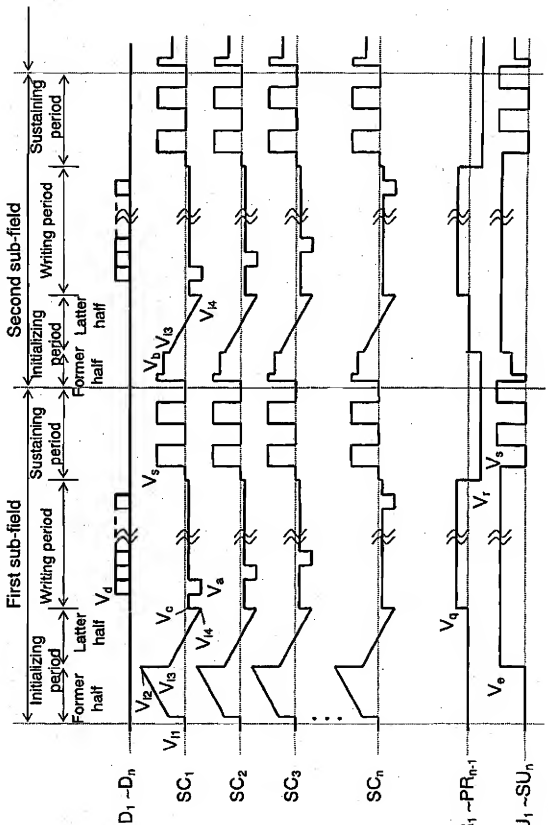

First sub-field
Second sub-field
Initializing period
Former half
Latter half
Writing period
Sustaining period
V_d
V_{f2}
V_{f3}
V_{f1}
V_c
V_{f4}
V_a
V_s
V_b
V_{f3}
V_{f4}
V_q
V_r
V_e
$D_1 \sim D_n$
SC_1
SC_2
SC_3
SC_n
$PR_1 \sim PR_{n-1}$
$SU_1 \sim SU_n$

FIG. 5

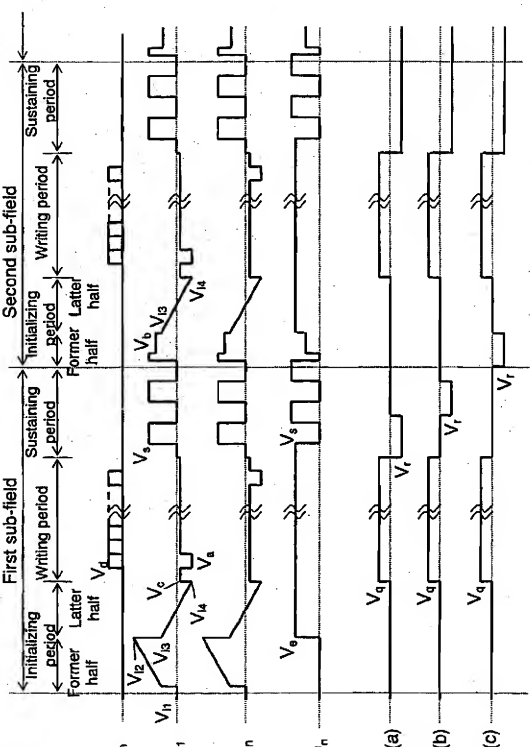
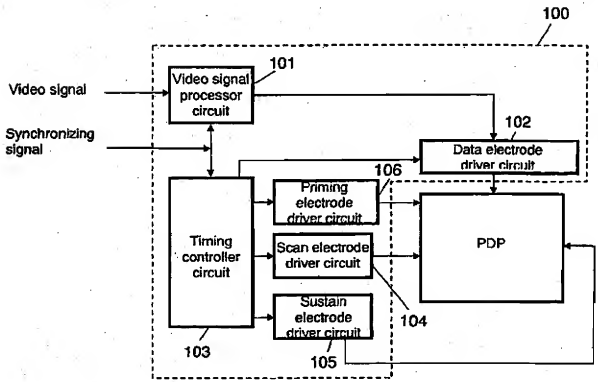

First sub-field
Second sub-field
Initializing period
Former half
Latter half
Writing period
Sustaining period
D_1~D_n
SC_1
SC_n
SU_1~SU_n
PR_1~PR_{n-1}
(a)
(b)
(c)
V_{f2}
V_{f3}
V_{f1}
V_{f4}
V_d
V_c
V_a
V_s
V_e
V_b
V_q
V_r

FIG. 6


100
101
Video signal
Video signal processor circuit
Synchronizing signal
102
Data electrode driver circuit
106
Priming electrode driver circuit
Timing controller circuit
Scan electrode driver circuit
PDP
Sustain electrode driver circuit
104
103
105

Reference marks in the drawings

1	Front substrate
2	Rear substrate
4	Dielectric layer
5	Protective layer
6	Scan electrode
6a, 7a	Transparent electrode
6b, 7b	Metal bus
6b'	Projection
7	Sustain electrode
8	Light-absorbing layer
9	Data electrode
10	Barrier rib
10a	Vertical wall
10b	Horizontal wall
11	Discharge cell
12	Phosphor layer
13	Clearance
13a	Priming space
14	Priming electrode
100	Driver
101	Video signal processor circuit
102	Data electrode driver circuit
103	Timing controller circuit
104	Scan electrode driver circuit
105	Sustain electrode driver circuit
106	Priming electrode driver circuit

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/003959

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/28, G09G3/20, H01J11/00-02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/28, G09G3/20, H01J11/00-02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Toroku Jitsuyo Shinan Koho	1994-2004
Kokai Jitsuyo Shinan Koho	1971-2004	Jitsuyo Shinan Toroku Koho	1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2001-185034 A (LG Electronics Inc.), 06 July, 2001 (06.07.01), Par. Nos. [0026] to [0034]; Figs. 5 to 7 & KR 2001038965 A	1-3
A	JP 8-96714 A (NEC Corp.), 12 April, 1996 (12.04.96), Par. Nos. [0039] to [0046]; Figs. 1 to 3 (Family: none)	1-3
A	JP 9-245627 A (Mitsubishi Electric Corp.), 19 September, 1997 (19.09.97), Par. No. [0065]; Fig. 19 (Family: none)	1-3

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 June, 2004 (21.06.04)	06 July, 2004 (06.07.04)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/003959

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5-313598 A (Fujitsu Ltd.), 26 November, 1993 (26.11.93), Par. Nos. [0016] to [0028]; Figs. 1 to 4 (Family: none)	1-3
A	JP 10-3281 A (Mitsubishi Electric Corp.), 06 January, 1998 (06.01.98), Par. Nos. [0035] to [0086]; Figs. 1 to 16 & KR 98004289 A & US 5854540 A	1-3